MICROMACHINED STIMULATING ELECTRODES

Quarterly Report #13

(Contract NIH-NINDS-N01-NS-5-2335)

October - December 1998

Submitted to the

Neural Prosthesis Program National Institute of Neurological Disorders and Stroke

National Institute of Neurological Disorders and Stroke National Institutes of Health

by the

Center for Integrated MicroSystems Department of Electrical Engineering and Computer Science

Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan
48109-2122

MICROMACHINED STIMULATING ELECTRODES

Summary

This program seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. During the past quarter, work has gone forward in a number of areas. We have continued to explore alternative processing options for defining the silicon substrate which shapes these probes, especially the use of an n+ buried silicon sacrificial layer. Such layers can be undercut in HF from the front at the end of the process so that the probes do not have to be released by etching completely through the wafer. We have evaluated this process using a mask set containing a 32-site active cochlear probe (ribbon cable) as a test vehicle. The probe was fabricated successfully with distributed electronics down the length of the 46mm shank. The probe contains 4 parallel current lines along with piezoresistors to allow the measurement of probe position inside the cochlea. The most difficult part of the process is the masking the HF release etch, and although present techniques are adequate for undercutting structures up to 500µm across, further development is needed in this area. The buried layer release approach remains a viable option for probe fabrication; however, the present boron etch-stop is useful in other ways, including suppression of substrate attack in saline, suppression of optical noise, and maintaining a low substrate resistance to avoid clock noise and crosstalk in stimulate-record situations. For now, the boron etch-stop will continue to be used for penetrating probe fabrication.

Titanium nitride has been reported to have a higher charge delivery capability than iridium oxide by at least one German group. We have developed the ability to sputter-deposit TiN at both normal and low-angle incidence and are studying the morphology of the resulting films along with their charge capacity and charge delivery characteristics. The results will be reported in the next quarterly report.

During the past term, the passive structural components necessary for the formation of 3D stimulating arrays using STIM-3B have been designed and fabricated. This includes several different platforms and accompanying spacers and cables. The resulting components will support the formation of arrays of up to 16x16 shanks and 1024 sites. In addition, passive prototype versions of the STIM-2/3 substrates have been fabricated. The new dielectric corner compensation technique has eliminated undercutting of the circuit areas and allows the reliable fabrication of short ribbon cables that should allow the circuit areas of these probes to lay flat against the cortex, resulting in a low implant profile. Fully-active stimulating arrays will be assembled during the coming term using the STIM-3B probes. Finally, the external user interface for the probes has been tested with additional STIM-2B probes and has been improved to allow more reliable operation. It is now being realized in printed-circuit-board form to support the efforts of active probe users.

MICROMACHINED STIMULATING ELECTRODES

1. Introduction

The goal of this research is the development of active multichannel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highlycontrolled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully and distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

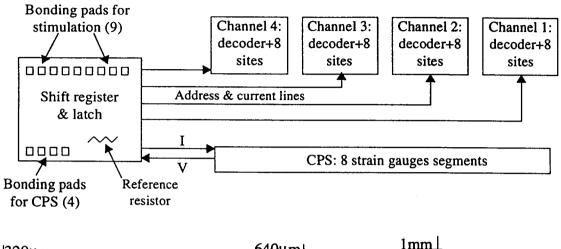
The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data which can be demultiplexed on the probe to provide access to a large number of stimulating sites. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into perchannel current amplitudes which are then applied to the tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now undergoing a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the perchannel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0µA to ±254µA with a resolution of 2µA, while STIM-2 has a range from 0 to $\pm 127\mu A$ with a resolution of $1\mu A$. STLM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STLM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, has now been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group, and the site can be programmed for either stimulation or recording. This probe is available in both 2D and 3D versions (as STIM-2B/3B).

During the past quarter, we have continued to fabricate passive probe structures for internal and external users. We have also continued to explore the use of an n+ buried silicon sacrificial layer for probe release as a possible alternative to the boron-diffusion process now used. This study has now been completed. TiN is also being studied as an alternative to iridium oxide as a site material. Finally, the platforms and spacers to form fully functional 3D arrays with the STIM-3B probes were successfully completed during the last term and are now ready for use in the formation of 3D arrays. Mock active STIM-2B/3B substrates have also been formed to test the feasibility of low-profile active cortical stimulating arrays. The external interface hardware for these probes has now been completed and debugged and is now being realized in a printed circuit board version. The results in each of these areas are described more fully in the sections below.

2. Development of a Sacrificial Bulk Micromachining Technology for Active Probe Fabrication

As outlined in previous quarterly reports, we have been exploring several process alternatives for use in defining the probe substrate to see whether they might offer significant advantages over the boron-diffusions that have become traditional in this role. The boron diffusion step is the least foundry compatible of all those used for probe fabrication. Even though it is offered commercially by some MEMS foundries, it is not commonly found in integrated circuit process foundries. The approach explored initially as an alternative to boron used a porous silicon layer, formed by electrochemically etching a p+ buried sacrificial silicon layer, to allow release of the probe structure without etching through the entire wafer. This release can be performed at room temperature, where the silicon etch does not significantly attack even exposed aluminum. More recently, we have found that the use of an arsenic-doped n+ buried layer is preferable for defining the substrate. This step avoids the outdiffusion problems associated with a p+ buried layer and avoids having to process the silicon after porous layer formation. Instead, an arsenicdoped buried layer is formed in the probe substrate early in the process. Arsenic has a much lower diffusion coefficient than boron and does not move significantly during subsequent processing. Epitaxial growth, planarization using a chemical-mechanical polish (CMP) (available commercially), and circuit fabrication then take place. After metallization and site formation, the probe is masked and subjected to a biased electropolishing etch in HF, which selectively removes the buried layer, releasing the probe from the wafer. This process is simpler than the process involving porous silicon; however, the release etch in HF is more difficult to mask than the porous silicon etch and requires that the probe area be capped with nitride and an appropriate HF mask. RIE is used to define the lateral extent of the probes. With either the p+ porous or the n+ electropolishing process, avoiding the long through-wafer etch is increasingly attractive as wafer sizes, and thicknesses, increase.

We have now completed our look at these alternative processes. As an application vehicle, a mask set which included 32-site active cochlear stimulating probes and 5-site passive recording probes was used. The cochlear probe was designed to allow stimulation of four channels simultaneously. Site selection is performed on-board, while the currents are generated externally. A series of eight polysilicon strain gauges were placed on the front-end insertable portion of the implant to measure bending of the substrate during and after insertion into the spiral cochlea. One of the eight gauges is selected at a time and its output compared differentially with a back-end reference resistor. Readings from the eight gauges can be used to form an image of the implanted substrate, allowing stimulus current levels to be adjusted for varying position in the cochlea. Figure 1 shows the overall design of the cochlear probe, while Fig. 2 shows the device cross-section.



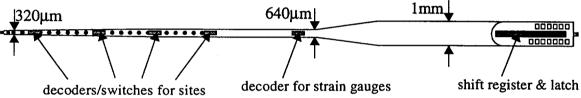


Fig. 1: Organization of the cochlear probe application vehicle for the use of an arsenic-doped buried layer in probe formation.

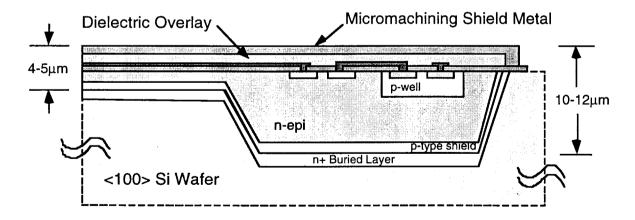


Fig. 2: Cross-section of a portion of a cochlear ribbon probe, used as a vehicle for exploring the use of an n+ buried sacrificial layer for probe release from the wafer. At the end of the process, the n+ layer is etched away, freeing the probe. The micromachining shield is then subsequently removed.

In fabrication, the substrate is first recessed to set the desired depths of the ribbon-cable sections and the circuit islands. Since the n+ buried layer process retains lightly-doped silicon for the probe shanks and circuit islands, demultiplexing circuitry can be distributed down the "shank" of the probe, reducing the number of leads required and, for a given width, allowing wider conductors and lower end-to-end interconnect resistances. After recessing the substrate, epitaxial silicon is deposited and planarized using CMP. The circuit process is executed followed by interconnect metal and site formation. Finally, the wafer is biased and placed in an HF etch to selectively undercut the buried layer. An example of the ability to undercut such a sacrificial buried layer is shown in Fig. 3.

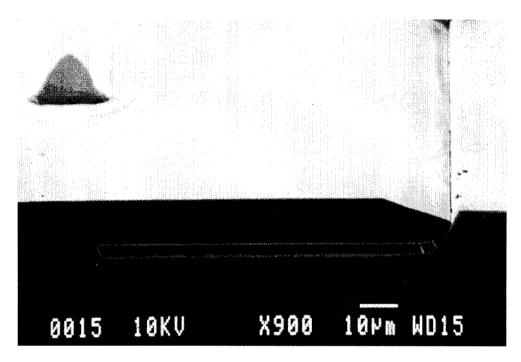
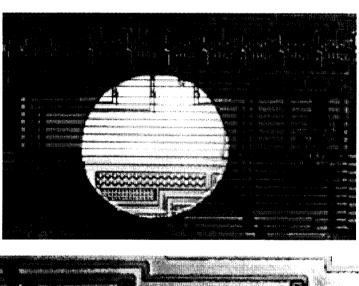


Fig. 3: Cross-section of an n+ buried layer under an epitaxial silicon region. The buried layer has been partially removed, illustrating the ability of a biased etch to selectively undercut a probe from the front of the wafer.

During the past quarter, these probes were fabricated. Figure 4 shows a top view of the circuitry on one of the distributed circuit islands. This circuitry was fully functional, as illustrated by the waveforms in Fig. 5. The only difficulties in the processing sequence were during the final release etch, where masking the HF was expected to be problematic. Our experiments have shown the ability to etch 1µm-thick n+ layers laterally at rates exceeding 10µm/min. Metal masks have been sufficient to protect the devices while undercutting lateral structures up to 500µm wide (from both sides); however, longer distances (etch times) resulted in excessive lifting of the Cr-Au mask. This performance is sufficient to undercut most ribbon-cable structures but is not sufficient to undercut the 640µm-wide cochlear probe completely. However, using etch-access slits (commonly used for enhanced flexibility on ribbon cables) at 200-300µm intervals, undercutting should be readily accomplished. We suspect that part of the etch-mask problems have come from the fact that when the metal etch mask overlaps the silicon substrate, it becomes biased, enhancing attack of the chromium layer under the gold. If the mask is arranged so that it remains on top of the dielectric, we expect masking will be less of a problem.

Our conclusion from this study is that an n+ buried layer can be used as a bulk sacrificial layer for front-side probe release. This process offers several advantages. Unlike the current boron process, it provides an etch-stop on all sides of circuit areas and, as a result, totally eliminates etch timing in release of the probes from the host wafer. It would also allow some circuitry to be moved from the back end of the probe to the shanks, decreasing the back end profile and enabling the number of sites to be increased without the number of leads increasing proportionally. This is especially important for 4.6cm-long cochlear implant probes, where wide leads are desirable to reduce voltage drops along the current lines. It also uses processes that are foundry standard (epi growth, CMP) and foundry compatible (electropolishing in HF) for the micromachining steps. However, the new buried-layer process is more complex than the boron etch-stop currently used. The epitaxial and CMP steps required are not currently available in our laboratory. In addition, the highly-doped boron substrate has other advantages. It also provides an etch stop to prevent the slow attack of the silicon substrate by biological fluids (saline) and reduces the minority-carrier diffusion length in the substrate to significantly reduce optically-generated noise and offsets. Further, it virtually eliminates the surface depletion layer in the substrate increasing the coupling capacitance to the extracellular fluid and lowering the bulk resistance of the substrate to suppress crosstalk.



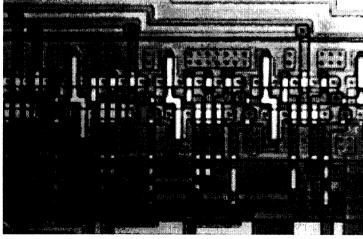


Fig. 4: Top view of the circuitry on a 32-site cochlear probe test vehicle. The top photo shows a view of the demultiplexing circuitry on one circuit island on the ribbon-cable probe along with a 250μ m-diameter stimulating site. The lower photo shows a closeup of the demultiplexing circuitry.

We have no plans to switch to the buried layer process at this time but will keep the process in reserve to be used as needed in the future. Some work will continue under other funding to explore this process further for a cochlear probe, where it is especially advantageous, and if the masking problems can be convincingly eliminated its use for CNS penetrating electrodes can be revisited in the future.

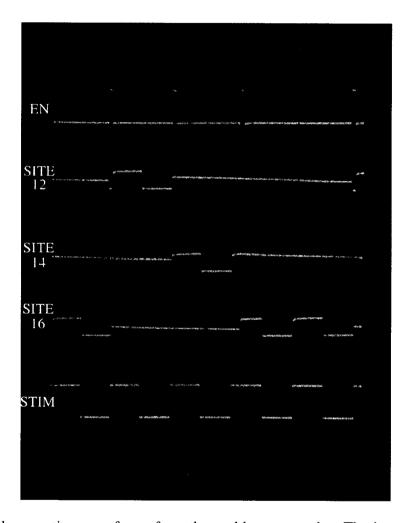


Fig. 5: Sample operating waveforms from the cochlear test probe. The lower waveform is the voltage applied to the input stimulus lead. The top enable signal is applied to the demultiplexers to load site addresses. Subsequent to each enable, a different site is selected and coupled to the stimulus. This was done to explore the feasibility of a bulk sacrificial process for probe fabrication, allowing the option of incorporating circuitry on the shanks and cables of the probes. This is particularly attractive for flexible cochlear devices.

3. Investigation of TiN as a Site Material

Titanium nitride is used extensively as a contact barrier material in integrated circuits and so is commonly available in most IC foundries as well as in our Laboratory. It is used as a passive barrier in the circuit contacts of all of our active probes. It is not clear when used as a site material what the injection mechanism is, but we have begun a serious look at

this material to explore its use as a possible alternative to iridium/iridium oxide. The German group at Reutlingen has has reported that while the charge capacity is less for TiN than for anodic IrO, the charge delivery capability is somewhat greater (by a factor of more than three). We are working to confirm this experimentally. Since the material, like iridium, is highly columnar in structure it may be that titanium in the grain boundaries can react with oxygen from the ambient to switch between different valence states (e.g., 2 and 4), much like iridium does. Sputtered at high pressures, the film is certainly porous and undoubtedly has a very high surface area. We do not know that it is safe when used for stimulation, but titanium is widely used as an implant packaging material (i.e., in pacemakers and drug pumps) and is thought to be safe chemically. We suspect that it is safe in stimulation as well so long as the excitation stays within the water window but the key question is what charge delivery is possible with this material in this range.

We have deposited TiN by sputtering at both normal incidence and at low-angle incidence. Figure 6 below shows a top view of the TiN surface, and Fig. 7 shows an impedance-frequency plot for this material. This was a large-area electrode (about 1cm²) so the spreading resistance in the solution becomes dominant at a different frequency than for a microelectrode. The curve indicates behavior typical of a polarizable metal electrode. CV tests show little if any growth in the charge capacity with continued low frequency cycling. The CV appears to open up for charge transfer primarily at the higher frequencies. The impedance is somewhat less than for iridium at these frequencies.

We are presently fabricating both recording and stimulating microprobes having TiN sites. These electrodes will first be used in further impedance spectroscopy and CV characterization and in acute in-vivo recording and stimulation tests. The potential advantage of TiN is a mechanically more stable film with high surface area and reasonable charge transfer at the frequencies used in stimulating systems. If our acute tests substantiate the Reutlingen data, we will use a chronic version of the probes in chronic experiments, where we can address the safety issues.

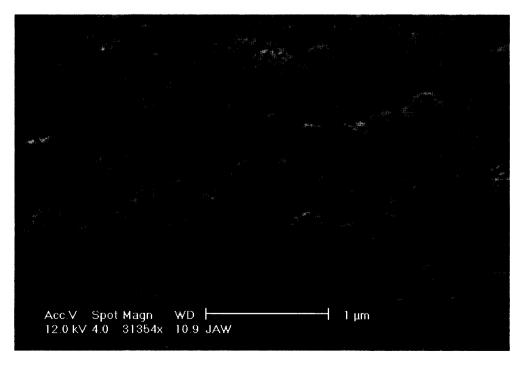


Fig. 6: Top view of the typical columnar structure of TiN sputtered at high pressure and normal incidence.

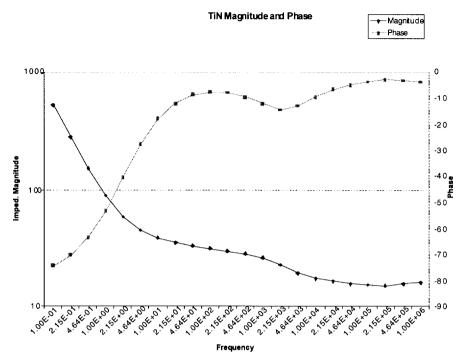


Fig. 7: Impedance versus frequency data for a large-area TiN electrode. The magnitude curve and consistent phase curve indicate typical polarizable electrode performance.

4. Active Stimulating Probe Development

During the past quarter, work on the active stimulating probes has focused on the fabrication of the structural pieces of the STIM-3B probe array (the 3D platform, cable, and spacers). These pieces have been successfully fabricated and etched out. Several test structures were also included in the same mask set to evaluate prototype probe structures for use in the high-end STIM-3 probe array which will include on-chip current generation. These structures have also been successfully etched out and the circuit areas have been shown to be well protected by properly designed and placed dielectric bridges even with integrated flexible ribbon cables which allow the back-end circuitry to be folded down to maintain a low implant profile above the cortical surface.

STIM-3B

STIM-3B is a 3-dimensional (3D) probe that is an extension of the 2D probe, STIM-2B, and is set up to allow use as a device in chronic experiments by virtue of a platform configuration with an integrated ribbon cable for connection to a percutaneous plug. There are no significant differences in the actual probe designs. The main differences are structural modifications to allow interconnection to a 3D platform assembly and a few minor circuit enhancements to facilitate addressing multiple probes in a 3D array.

The functionality of the STIM-3B probe is expected to provide an important tool for performing some very important and interesting experiments by allowing acute and chronic stimulation access to a relatively large volume of neural tissue without mechanically repositioning the probe. As in the STIM-2B design, the STIM-3B probe is a four-channel,

16-shank, 64-site probe which routes four externally generated stimulus signals to 1-of-16 sites per channel. This capability is realized by utilizing a 20b shift register to load four 4b site addresses, which are decoded by a 1-of-16 nand-type decoder to connect the desired site to an analog input/output pad through a large CMOS passgate transistor, thereby allowing the *steering* of externally generated stimulus currents to the addressed site. A simple recording function has been included and is addressed by a fifth bit included with the 4b site address. This fifth bit selects between stimulation mode and recording mode by selecting either a direct path to the I/O line from the site or a path through an amplifier for recording from the same site. Each I/O channel has its own dedicated amplifier so that the functionality of all of the channels is independent of each other except for the up-front data input circuitry.

In order to allow addressing of multiple probes in a 3D array, STIM-3B has an extra 4b serial input shift-register which, when the bits are set, connects the corresponding I/O channel of the probe to a common I/O bus on the platform. All of the extra registers of the probes in a STIM-3B array are connected in series via platform leads to form an extended or virtual register. The virtual register enables all of the probes of a 3D array to be addressed with only two address lines: a channel enable address line and a site address line. This architecture does have a limitation in that it does not allow independent use of the same site address on two separate probes in the array. The slightly reduced flexibility was considered a reasonable sacrifice to achieve a reduction in circuit complexity and, more importantly, lead count.

Rather than waste area on the active CMOS probe mask set, the STIM-3B 3D structural pieces were designed on a completely separate mask set, which only required six masks and was essentially the same fabrication process as is used for passive probes. The only difference is that there are no site or pad masks; instead, there is a single beam/pad electroplating mask. The electroplating mask is used as the final step to form the beam lead interconnects and pads on the platforms after the field etch has been done. The conductor mask was designed with the polarity reversed from what it would normally be for a passive probe so that it could be used in a lift-off process for metal conductors instead of polysilicon. The first wafers that have been completed still use polysilicon (patterned by image reversal) and the normal high temperature dielectrics, but we intend to complete other wafers, left back in the fabrication process, using lower resistance conductors and therefore different upper dielectrics.

Four different platform designs were included on this mask set, of which two are shown in Fig. 7 and one in Fig. 8, all on a wafer just prior to the EDP release etch. The designs include three platforms that can be programmed by selectively blowing integrated microfuses with a current pulse to hold up to four probes. Two of the designs have all the probes facing the same direction and differ only in how the ribbon cable exits the platform: one from the narrow edge of the platform, as shown in the top of Fig. 7, and the other from the wide edge of the platform (not pictured, but seen in Fig. 10). The third platform design, shown in the bottom of Fig. 7, is such that all of the probes face the centerline of the platform. The last design is the largest platform that we have ever fabricated; it can be programmed to hold up to 16 probes. When fully populated, the platform will hold a 16x16 array of four-site shanks creating a 3D grid of 1024 stimulating sites on 400µm centers spanning 1.2mm x 6mm x 6mm or a volume of 43.2mm³. An enlargement of some of the electroplated gold pads and interconnects on a platform and the electroplated gold beam leads on the connector are shown in Fig. 9. One of the microfuses is also indicated in the picture. The microfuse is simply a bridge of electroplated gold suspended over a pit formed by etching out exposed polysilicon during the EDP release etch.

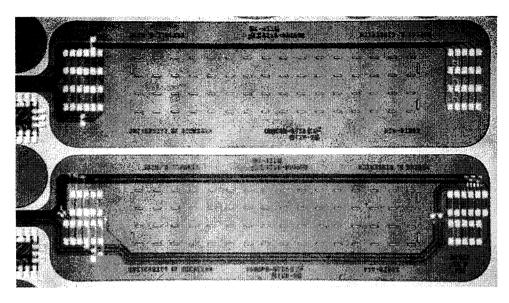


Fig. 7: A photograph of two of the platform designs that can be programmed via microfuses to hold up to four probes each. The top platform holds all the probes in the same direction while the bottom platform is designed such that all the probes face the centerline of the platform.

The platforms and the associated spacers and handling discs (which are placed on top of an assembled array for vacuum-pick handling) have been successfully etched out and some are shown in Fig. 10 along with one of the STIM-3B active probes. There is some curvature in the ribbon cables due to a small stress mismatch in the dielectric layers. All of the pieces for a 3D active stimulating array are now ready for assembly.

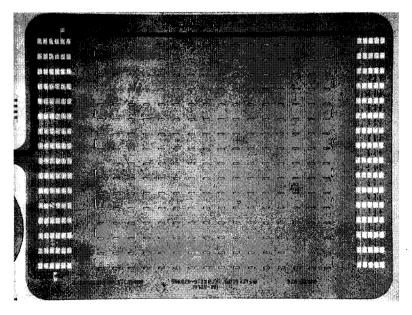


Fig. 8: A photograph of the largest platform design, which can be programmed via microfuses to hold from one to sixteen probes at maximum, creating a 16x16 array of four-site shanks on 400µm centers for a total of 1024 stimulating sites.

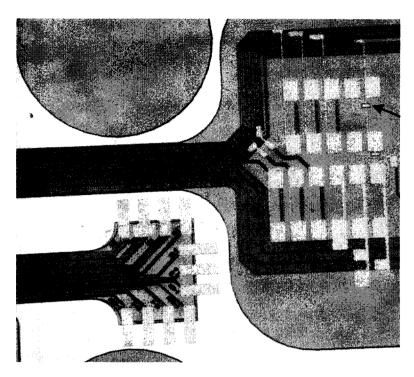


Fig. 9: A photograph showing a close-up of some of the electroplated gold interconnects and pads on a platform and the beam leads on the connector end of a ribbon cable. The position of one of the platform's microfuses is also shown.

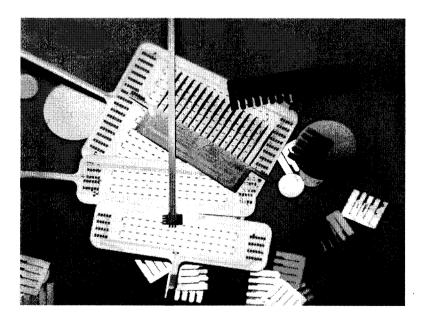


Fig. 10: A photograph of several of the etched-out platform designs, spacers, and a STIM-3B probe. The platform design not previously shown can be seen at the bottom with the ribbon cable extending from a wide edge.

STIM-3 Test Structures

STIM-3 will be a high-end active CMOS 3D stimulation array with on-chip current generation, minimal lead count, low profile, and up 1024 sites. In order to prepare for the design and fabrication of this system, several test probe structures were included on the STIM-3B 3D platform mask set. These structures were intended to test the feasibility of folded-down circuitry on a probe for reduced height of a 3D probe array. The structures were also intended to test how well the circuit area could be protected from undercut using properly designed dielectric bridges. Figure 11 shows one of the test probe structures. Dielectric bridges are included at the corners of the back-end circuit area in order to protect them from undercut. Multiple dielectric bridges are also included between the flexible interconnects in order to provide protection for the front edge of the circuitry, which in the past has been susceptible to undercut due to the early breakthrough of the backside etch plane in the wider areas between the shanks or in this case the flexible interconnects. The dielectric bridges between the flexible interconnects may or may not break off, but it does not matter in this case. Four different test structures were included: one with long straight flexible interconnects, one with short straight flexible interconnects, one with long angled flexible interconnects, and one with short-angled flexible interconnects. The different variations were included in order to test if either the straight or the angled flexible interconnects would etch out better and to test if there is one configuration that folds down the best. Three of the etched out structures are shown in Fig. 12. As it turns out, all of the different configurations etch out quite well. The etch-out test has shown that the circuit area remains well protected even with a significant over-etch (nearly 1/2 hour), as can be seen by the thick silicon area on the backside of the probe as indicated in Fig. 12. The even width of undercut around the circuit area shows that the front side is now also well protected by the multiple dielectric bridges, even though the flexible interconnects are quite far apart. All the rest of the structure has been cleared to the boron etch stop as it should be; this was true for all four configurations. At this point none of the structures appears to be any better than the others, but that may change when we insert the structures into a platform and look at the issues of folding the circuit area down. This will obviously only be done using platforms that are defective and therefore not useful for functional 3D arrays.

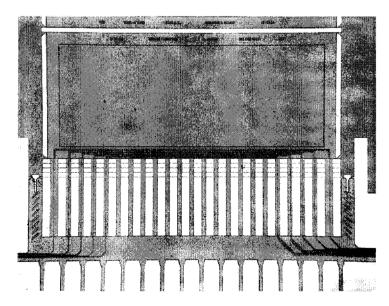


Fig. 11: A photograph of one of the structures for testing the fold-down design of STIM-3B using flexible ribbon cable interconnects as well as the technique for protecting the circuitry from undercut using dielectric bridges.

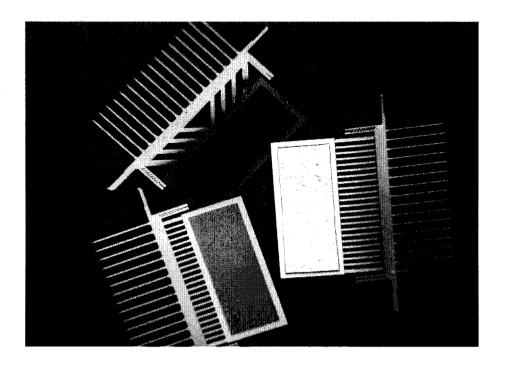


Fig. 12: A photograph of etched-out STIM-3 test structures. Three configurations are shown with the one on the right having its backside turned up, showing the protected thick silicon circuit area.

In summary, the STIM-3B 3D array structural pieces for the four different platform configurations have been fabricated, so all of the pieces of the 3D arrays are now ready for assembly. The test structures for the high-end STIM-3 array design have been successfully etched out demonstrating the circuit protection scheme and are ready for use in testing the folded-down-circuitry concept for reducing the array profile. During the coming quarter, we anticipate assembling STIM-3B 3D arrays, and we then plan to conduct *in-vitro* and *in-vivo* testing. We anticipate completing the fabrication of more arrays utilizing a lower resistivity conductor material for improved array performance. We plan to perform the assembly and testing of the folded-down-circuit scheme for 3D array profile reduction. Testing of the STIM-2B probes is ongoing, and we plan to utilize the design in more significant *in-vivo* experiments with the capabilities of the PC based external user interface system. With the results of the structure tests, the design of the high-end 3D STIM-3 array will move toward completion to realize more advanced arrays of up to 512 or 1024 sites.

5. An External Interface to Micromachined Stimulating Probes

In previous reports, we have described the design and construction of a hardware and software system to support an interface to active stimulating probes. During the past quarter, we attempted to use our external stimulating system prototype to support *in vivo* stimulation experiments. Previous integration tests between the external system and stimulating probes were successful, and we expected no problems. For this round of testing, however, we were unable to drive the stimulating probe with the external system.

As the first probes tested were no longer available, we were unable to return the known-good system.

We have investigated the interface problem and believe we have discovered the root causes. There were three significant issues:

- 1. The external hardware system contained a wiring problem which generated a very poor -5V supply voltage. Although the static voltage level appeared normal on a voltmeter, the supply had minimal current capacity and would become severely loaded while driving into the probe inputs. This led to degrading effects such as time-varying ground levels.
- 2. The use of a six-foot unshielded serial cable to deliver the probe signals from the external system to the probe led to slightly noisy signals. More importantly, a fair amount of capacitive coupling between the clock and data line was observed. Thus, just as the clock signal was falling to latch in the data signal, the data signal suffered a glitch. This glitch resulted in unreliable interpretations of the data signal value.
- 3. The rise and fall times of the clock signal were found to be too slow. The slow rise time overshadowed the built-in delays of the probe that are used to ensure the latch cells retain their value before driving the on-board multiplexers. This effect led to unreliable operation, in which a certain signal pattern only intermittently achieved the desired effect.

The above problems were easily fixed. The poor -5V supply voltage was replaced with an external power supply. The clock and signal lines were routed from the external system to the probe using separate shielded cables. Finally, the analog output drivers on the external system were given lower output impedances, reducing the rise and fall times and sharpening the transitions. The first two changes were artifacts of the prototype implementation, while the last change was a minor modification to the design. After implementing these changes, we verified the operation of the external system with two different probes and over several different stimulating sites. We are now confident that the two systems will reliably interoperate in the future.

This experience improved our knowledge of the electrical characteristics of both the probe and the external system. It also indicated that the final system design should include a connector for a shielded cable rather than the simple unshielded cable in the original design.

The remaining tasks for the external system development are the realization of the design on a printed circuit board and hardware/software documentation. The former task is nearly complete. The electrical components for the circuit board have been procured, although a handful of parts are on backorder. Once all parts have arrived, the design will be submitted for manufacture with an expected turnaround time of three weeks. The task of documenting the hardware and software designs is in progress and will be completed by the end of the coming quarter.

6. Conclusions

This program seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. During the past quarter, work has gone forward in a number of areas. We have continued to explore alternative processing options for defining the silicon substrate which shapes these probes, especially the use of an n+ buried silicon sacrificial layer. Such layers can be undercut in HF from the front at the end of the process so that the probes do not have to be released by etching completely through the wafer. We have evaluated this process using a mask set containing a 32-site active cochlear probe (ribbon cable) as a test vehicle. The probe was fabricated successfully with distributed electronics down the length of the 46mm shank. The probe contains 4 parallel current lines along with piezoresistors to allow the measurement of probe position inside the cochlea. The most difficult part of the process is the masking the HF release etch, and although present techniques are adequate for undercutting structures up to 500µm across, further development is needed in this area. The buried layer release approach remains a viable option for probe fabrication; however, the present boron etch-stop is useful in other ways, including suppression of substrate attack in saline, suppression of optical noise, and maintaining a low substrate resistance to avoid clock noise and crosstalk in stimulate-record situations. For now, the boron etch-stop will continue to be used for penetrating probe fabrication.

Titanium nitride has been reported to have a higher charge delivery capability than iridium oxide by at least one German group. We have developed the ability to sputter-deposit TiN at both normal and low-angle incidence and are studying the morphology of the resulting films along with their charge capacity and charge delivery characteristics. The results will be reported in the next quarterly report.

During the past term, the passive structural components necessary for the formation of 3D stimulating arrays using STIM-3B have been designed and fabricated. This includes several different platforms and accompanying spacers and cables. The resulting components will support the formation of arrays of up to 16x16 shanks and 1024 sites. In addition, passive prototype versions of the STIM-2/3 substrates have been fabricated. The new dielectric corner compensation technique has eliminated undercutting of the circuit areas and allows the reliable fabrication of short ribbon cables that should allow the circuit areas of these probes to lay flat against the cortex, resulting in a low implant profile. Fully-active stimulating arrays will be assembled during the coming term using the STIM-3B probes. Finally, the external user interface for the probes has been tested with additional STIM-2B probes and has been improved to allow more reliable operation. It is now being realized in printed-circuit-board form to support the efforts of active probe users.